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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/801,819	03/17/2004	Teru Yoneyama	Q80332	2517
23373 7590 01/18/2008 SUGHRUE MION, PLLC 2100 PENNSYLVANIA AVENUE, N.W. SUITE 800 WASHINGTON, DC 20037			EXAMINER SHAPIRO, LEONID	
			ART UNIT 2629	PAPER NUMBER
			MAIL DATE 01/18/2008	DELIVERY MODE PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

## Office Action Summary

**Application No.**

10/801,819

**Applicant(s)**

YONEYAMA, TERU

**Examiner**

Leonid Shapiro

**Art Unit**

2629

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 17 March 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,2 and 7-12 is/are rejected.
- 7) ☒ Claim(s) 3-6 and 13-20 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1-2,7-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Aizawa (US 5,796,767).

As to claim 1, Aizawa teaches a current drive circuit (col. 1, lines 6-8) comprising:

a current mirror circuit (fig. 4, items Q1-Q2,Q5, col. 6, lines 53-57);

a current source for applying reference current input to said current mirror circuit (fig. 4, item 4, col. 6, lines 39-45);

a switch means to which output current of said current mirror circuit is applied (fig. 4, items 2,Q7-Q8, col. 6, lines 58-67); and

a cascode circuit for supplying the output current of said switch means as a drive current (fig. 4, items Q3-Q8, col. 6, lines 46-52).

As to claim 2, Aizawa teaches a current drive circuit (col. 1, lines 6-8) comprising:

a bias generator that includes:

a first transistor in which a gate terminal and a drain terminal are connected together (fig.14, item Q3);

a second transistor in which a source terminal is connected to said

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drain terminal of said first transistor and a gate terminal and a drain terminal are connected together (fig.14, item Q4); and

a current supply that causes a reference current to flow to said second transistor (fig.14, items 4,Q4); and

a current output unit that includes:

a third transistor in which a gate terminal is connected to said gate terminal of said first transistor (fig.14, item Q7);

a fourth transistor in which a gate terminal is connected to said gate terminal of said second transistor (fig.14, item Q8); and

a switch means that is provided between a drain terminal of said third transistor and a source terminal of said fourth transistor (fig.14, item Q9).

As to claims 7-8, Aizawa teaches switch means is turned ON and OFF by a control signal (fig. 14, item 3).

As to claims 9-10, Aizawa teaches a graduation signal (fig. 14, item DT).

As to claims 11-12, Aizawa teaches MOS transistor (col. 6, lines 46-52).

### ***Allowable Subject Matter***

2. Claims 3-6,13-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Relative to claim 3 the major difference between the teaching of the prior art of

record (Aizawa) and the instant invention is that a plurality of said current output units; and a plurality of terminals that are connected to each of drain terminals of said fourth transistors of said plurality of said current output units.

Claims 4,13,15,17 depend on claim 3.

Relative to claim 3 the major difference between the teaching of the prior art of record (Aizawa) and the instant invention is that a plurality of current drive circuits; and a terminal that is connected to drain terminals of each of said fourth transistors of said plurality of said current drive circuits.

Claims 6,14,16,18 depend on claim 5.

Relative to claim 19 the major difference between the teaching of the prior art of record (Aizawa) and the instant invention is that organic EL elements that are arranged in a matrix; current drive circuits and scan circuits for causing drive currents to flow to said organic EL elements; and signal processing circuits for receiving image data signals as input, supplying graduation data signals to said current drive circuits, and supplying scan control signals to said scan circuits.

Relative to claim 20 the major difference between the teaching of the prior art of record (Aizawa) and the instant invention is that organic EL elements that are arranged in a matrix;. current drive circuits and scan circuits for causing drive currents to flow to said organic EL elements; and signal processing circuits for receiving image data signals as input, supplying graduation data signals to said current drive circuits, and supplying scan control signals to said scan circuits.


***Telephone Inquire***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonid Shapiro whose telephone number is 571-272-7683. The examiner can normally be reached on 8 a.m. to 5 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Hjerpe can be reached on 571-272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

LS  
01.17.08



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SUPERVISOR PATENT EXAMINER  
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